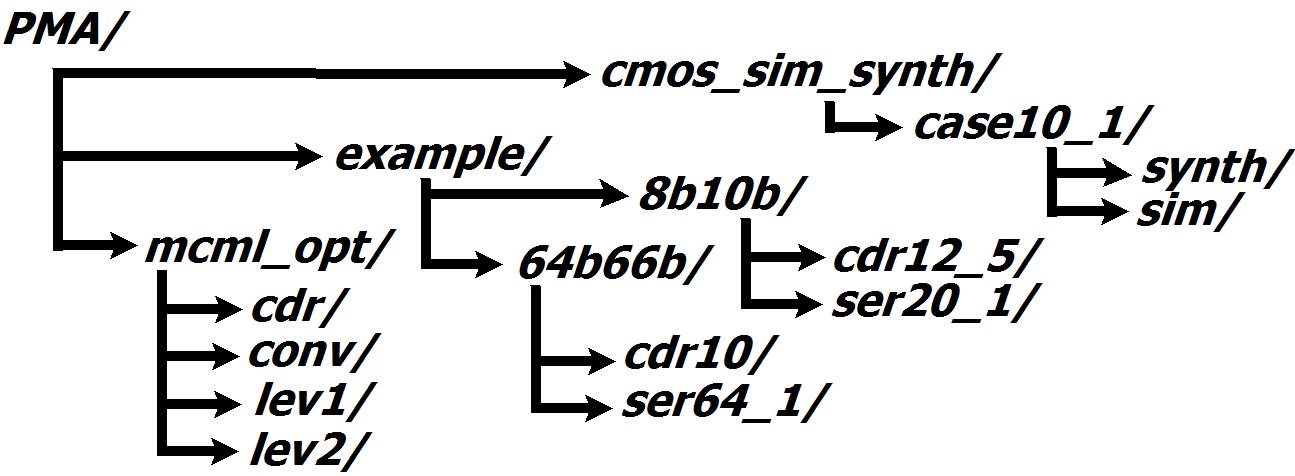
**Code structure PMA/**

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**Physical Medium Attachment**

Physical Medium Attachment sublayer provides a bridge between encoding blocks, such as given by 8b10b and 64b66b PCSs, and the high-speed serialization/deserialization (SerDes) units of a transmitter by converting the low-speed parallel data into a high-speed serial bit stream. Two different PCS sublayers impose the use of different SerDes blocks operating at different speeds. In particular 64b66b coder produces parallel 64bit sequences at 161.13MHz, transferring them to a 64:1 serializer. The line rate of a serialized stream is 10.3125Gbps, which corresponds to the rate provided by a standard Ethernet 10GBASE-R PHY [1]. In contrast to that, 8b10b coder, depending on the PCS design, can perform either 10:1 or 20:1 data multiplexing, supporting the line rate of 12.5Gbps due to a higher overhead of 8b10b code. The top-level representation of PMA sublayer is given in Figure 1.

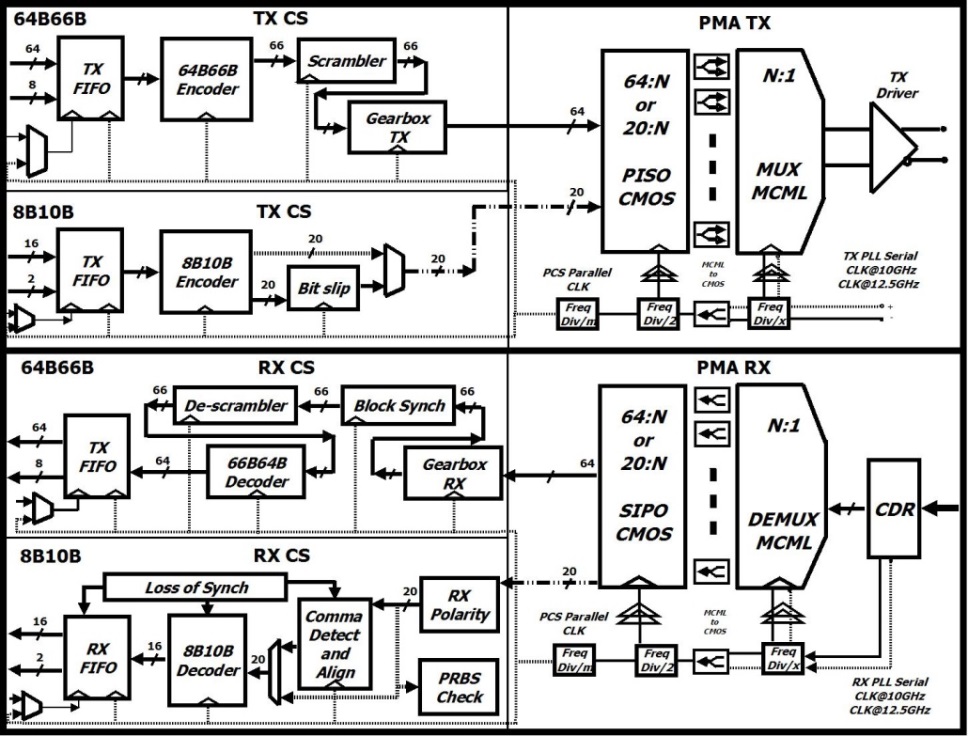


Figure 1. Top-level diagram of the transceiver design

**SerDes design**

The variation in CS block design imposes the use of different SerDes blocks operating at different speeds and datawidth conversion ratios. 64B66B coder implementation transfers parallel 64bit sequences, resulting in the 64:1 serializer design. A typical SerDes unit can incorporate both static CMOS Parallel-In-Serial-Out/Serial-In-Parallel-Out (PISO/SIPO) data conversion and a differential Current Mode Logic (CML) tree-based multiplexer/ demultiplexer (MUX/DEMUX) designs for better noise immunity.

**Static CMOS SerDes**

Static CMOS Serialization/Deserialization blocks are synthesized in automated way using commercially available 45nm technology process library and Synopsys tools. The typical clock frequency margin used for the synthesis is considered to be at least 15% higher than the nominal frequency value; the uncertainty values for setup and hold times, and, the crude delays on elements composing clock and data distribution networks were extensively specified to meet the timing objectives of design synthesis at high operating speeds.

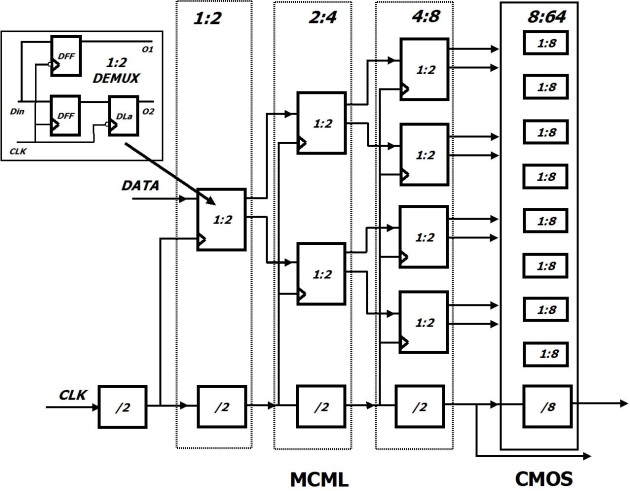
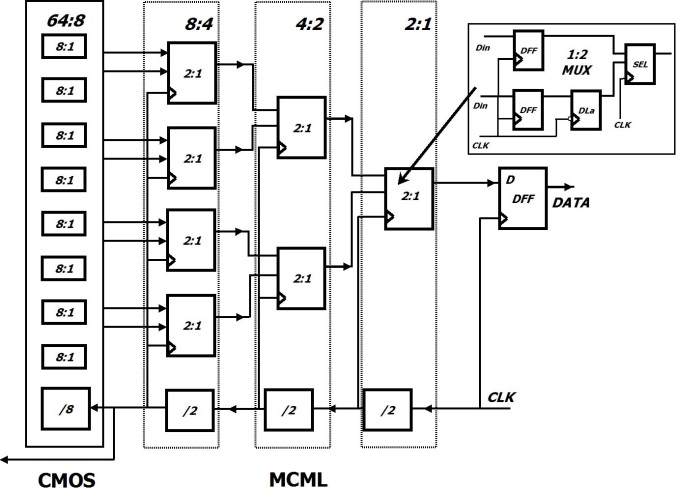
****SerDes (Figure 2) operation at line-rate transmission frequencies introduces a certain noise and power scaling challenges if realized with standard CMOS libraries. The noise factor limits the on-chip integration of digital blocks with their analog counterparts, while the accuracy of circuits’ operation is eminently affected. New logic families, such as differential MOS Current Mode Logic (MCML) [2, 3, 4] help to overcome these issues. The differential signal nature relaxes the high-speed operation, guarantees the minimal noise penalties and power independence on the input stimuli applied.

Figure 2.(a) A 64:1 MUX block diagram. (b) A 1:64 DEMUX block diagram.

**MCML tree-based SerDes**

The MCML library development process involves the use of transistor models supplied with standard CMOS process libraries and a semi-analytical methodology developed in HSPICE environment for cells optimization. To satisfy the required performance criteria of high-speed operation and minimize power dissipation of individual gates, a built-in HSPICE optimization solver was used; this allowed producing the best case parameter variation model for a specific subset of supply voltages, voltage swings and biasing currents selected as the input characteristics.

The effect of various SerDes ratios is shown in Figure 2, for example, for 64b66b we consider a 64:8 CMOS circuit combined with 8:1 MCML circuit to achieve the 64:1 SerDes functionality (henceforth called the 64:8:1 case). In general large variations of implementations are possible (for instance, 64:4:1, 64:2:1 and other cases) depending on design requirements. It can be observed that the optimum ratio depends on the input frequency, with a 20:2:1 ratio being optimum for 16b/20b transceivers with a 625 MHz input frequency, and 10:2:1 for 8b10b transceivers with 1.25GHz parallel input frequency.

**CDR design**

In order to avoid significant penalties and delays due to the clock recovery process, a single stage Clock and Data Recovery (CDR) circuit was designed. The proposed architecture is shown in Figure 3 aims at reducing power consumption and provides fast locking mechanism for speedy clock phase compensation and regeneration. Commonly used PLL and CDR circuits often use multiple stages in order to facilitate a stable and consistent operation. This redundancy usually delivers high performance but the synchronization process takes a relatively long time to achieve a stable lock. The simplicity of the provided CDR design guarantees a relatively fast locking time (<10 clock cycles), good power-efficiency as well as good on-chip integration possibilities. The design was synthesized in hardware by means of the standard cell library components(gates), a set of passive components, used in LPF design, and, a MCML-based ring oscillator [3], designed from the previously described MCML cell library.

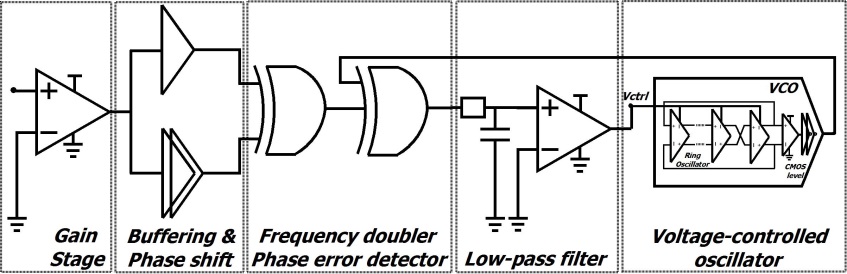


Figure 3.Clock and Data Recovery circuit

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[1]. IEEE 802.3ae. Part of IEEE Std 802.3-2008 (<http://www.ieee802.org/3/>).

[2]. M. Yamashina and H. Yamada, “An MOS current mode logic (MCML) circuit for low-power sub-GHz processors,” *IEICE Transactions on Electronics*, vol. 75, no. 10, pp. 1181-1187, 1992.

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